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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,877	03/19/2004	William David Llewellyn	08211/0200389-US0/P05835	7655
38845	7590	04/18/2007		
DARBY & DARBY P.C. P.O. BOX 5257 NEW YORK, NY 10150-5257			EXAMINER KING, SONIA J	
			ART UNIT	PAPER NUMBER
			2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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Office Action Summary	Application No. 10/804,877	Applicant(s) LLEWELLYN ET AL.	
	Examiner Sonia J. King	Art Unit 2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 August 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>6/01/2004</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claim 1 rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai JP 409063206 A in view of Yasuda JP35906893 A, in further view of Castiglione et al US 7079616 B2, and in view of Davis US 5907253, an in addition in view of Chang US PG Publication 2002/0145478 A1.
3. With respect to claim 1, Sakai teaches a circuit for spread spectrum clock generation, comprising: a phase detection circuit that is configured to provide an error signal from a reference signal (regenerative signal); a voltage controlled oscillator circuit that is configured to provide a synthesized signal from the error signal; (Abstract) The phase error is detected from the regenerative signal before waveform equalized outputted from a low pass filter by an analog clock phase error detection circuit. The benefit being that by imparting the synthesized signal to a voltage controlled oscillator as a control signal through a loop filter, the initial pull-in operation of the identifying clock phase is performed.
4. Sakai fails to teach a feedback signal is also configured by the phase detector as claimed. However, Yasuda does teach this feature in the Abstract. The benefit being that the output of the carrier oscillator and the feedback signal are synthesized so that

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an input phase is automatically compensated and an output phase can also be compensated.

5. Therefore taking the combined teaching of Sakai and Yasuda as a whole, it would have been obvious to modify the phase detection circuit of Sakai to include the feedback signal as taught by Yasuda as in the claimed invention. Thus enabling the whole system to automatically compensates the input and output phase.

6. The combined teaching of Sakai and Yasuda fails to teach a modulating waveform generator circuit that is configured to provide a modulating waveform signal that varies over time as a modulating waveform as claimed. However, Castiglione et al does teach this feature in Figure 1. According to Castiglione, the phase locked loop also includes a feedback path that is responsive to the signal generated by the oscillator and which generates said feedback signal via least one divider with a variable division ratio. The division ratio of said divider is modulated via a sigma-delta modulator, the input of which is fed with a triangular-wave modulating signal. (Abstract) The advantage being that a triangular "cusp-like" modulating signal is used in an attempt to improve the borders of the clock's spread spectrum. (Column 2 lines 14-16)

7. Therefore, taking the combined teaching and Castiglione as a whole, it would have be obvious to one of ordinary skill in the art at the time of the invention, to modify the combined teaching to include modulating waveform generator circuit that is configured to provide a modulating waveform signal that varies over time as a modulating waveform as taught by Castiglione. Thereby enabling the whole system to

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provide a triangular "cusp-like" modulating signal in an attempt to improve the borders of the clock's spread spectrum.

8. The combined teaching fails to teach an accumulator circuit that is configured to provide a carry signal from the modulating waveform signal as in the claimed invention. However, Davis et al does teach this feature in Figure 6. According to Davis, the carry output of the accumulator serves as the modulus control signal M for the counter and instructs the counter to add the one additional count when more than one full voltage controlled oscillator period of phase lag has accumulated (there by preventing the variable delay gate range from being exceeded). The summation signal is also used to increment the delays within the delay element. (Column 2 lines 11-18) The advantage being that the self-calibration of the fractional delay element within the DLL requires only one comparator. This eliminates the need for multiple signal comparison thresholds which, in turn, eliminates reference frequency related signal spurs in the output due to mismatches within the comparison circuits. Moreover, phase comparisons can be performed at a faster rate which can be established independently of the period of the voltage controlled oscillator output signal. This results in the phase locked loop spending less time in an uncertain state which, in turn, results in less output signal phase noise. (Column 3 lines 22-31)

9. Therefore, taking the combined teaching and Davis as a whole, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined teaching to include the accumulator circuit configured to provide a carry signal from the modulating waveform signal as taught by Davis so that the whole

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system would spend less time in an uncertain state and have less output signal phase noise.

10. The combined teaching fails to teach an adjustable clock divider circuit as claimed. However, Chang does teach this feature in Figure 4. According to Chang, an adjustable clock divider circuit that is configured to provide an adjustable clock divider output signal (V_{c1}) from an adjustable clock divider input signal (F_{ref}), wherein the adjustable clock divider input signal is based at least in part on the synthesized signal (V_c), the feedback signal (F_{vco}) is based at least in part on the adjustable clock divider output signal (V_{co2}), and wherein the adjustable clock divider circuit is configured to provide the adjustable clock divider output signal such that a frequency that is associated with the adjustable clock divider signal corresponds to the frequency associated with the adjustable clock divider input signal divided by: a first number (N), if the carry signal is associated with a first logic level, and a second number (M), if the carry signal is associated with a second logic level. The circuit includes a first voltage-controlled oscillator (VCO) that generates a feedback clock. The circuit further includes a phase frequency detector, a charge pump and a loop filter that together receive a reference clock and the feedback clock and in response generates a first voltage signal.

[paragraph 0014] The phase locked loop circuit of the invention includes a N-divider 12, a M-divider 14, a phase frequency detector 16, a charge pump 18, a loop filter 20, a voltage modulator 30, a FM/AM timing generator 40, and voltage-controlled oscillators (VCO) 22 and 24. [paragraph 40] the voltage modulator 30 in the phase locked-loop circuit generates a first control voltage V_{c1} , and a second control voltage V_{c2} that

varies periodically. The first VCO 22 received the first control voltage V_{c1} and generates a stable feedback clock F_{vco} . The second VCO 24 receives the second control voltage V_{c2} and generates a spread spectrum clock F_{vco2} . The structure of the first VCO 22 and the second VCO 24 can be the same. A timing control signal is generated from the FM/AM timing generator 40 for controlling the voltage modulator 30 to generate the second control voltage V_{c2} that varies periodically. [paragraph 41] The advantage being that since only one loop is used the phase locked loop circuit is simple and easy to maintain stable [para 0016]. The frequency range of the spread spectrum clock can be quantified, and the frequency of the spread spectrum clock can be controlled in a programmable way [para 0017]. The time of frequency variation can be quantified, and is programmable, the energy can be spread over a much wider range [para 0018]; and since the frequency of the spread spectrum clock varies periodically, there will be no constant frequency, no surge will be generated, and the spread spectrum clock will be uniform. [para 0019]

11. Therefore, taking the combined teaching and Chang as a whole it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined teaching to include adjustable clock divider circuit as taught by Chang so that the entire system would be simple and easy to maintain, the energy can be spread over a much wider range and the spread spectrum clock will be uniform.

12. As to claim 2 and 15, refer to the combined teaching wherein the second number equals the first number minus one. Note also the details of Figure 6 in Davis, wherein it

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teaches $N=n$ and $M=n+1$. Therefore it would have been obvious to one of ordinary skill in the art that if $M=n+1$ it is also the opposite is also true.

13. Claim 3 rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teaching as applied to claim 1 above, and further in view of Jeon US PG Publication 2003/0058053 A1

14. As to claim 3 the combined teaching above fails to teach that the modulating waveform is suitable for reducing electromagnetic interference as claimed. However, Jeon et al does teach this feature in Figure 4. According to Jeon, the phase locked-loop for reducing the EMI controls the signals having phase difference, which is n -times (where n is an integer) the basic delay time of the output signals from a voltage controlled oscillator (VCO), and determines the modulation rate. Then, the phase locked-loop repeats the procedure during the cycle of a pre-defined modulation frequency. The advantage being that the phase locked-loop for reducing the EMI not only reduces the EMI, but also does not require a ROM. Thereby, the layout space can be reduced and broad frequency ranges can be obtained. Also, since the phase difference of the output signals of the VCO is controlled by logic circuits, the PLL is insensitive to changes in the manufacturing process. (Abstract)

15. Therefore, taking the combined teaching and Jeon as a whole, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined teaching to include the phase-locked loop circuit capable of adjusting the frequency range of spread spectrum clock as taught by Jeon so as to enable the whole system to be able to reduce the electromagnetic interference as in the claimed

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invention. In so doing, a circuit that consumes less power, occupies a small layout space and can flexibly control a modulation frequency and a modulation rate flexibly is provided.

16. Claims 4 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teaching as applied to claim 1 above, and further in view of Prockup US 6760571 B2.

17. As to claim 4 refer to the combined teaching above. Note also, that Castiglione does teach the modulating waveform includes one of a triangle wave as disclosed in Figure 1. Castiglione fails to teach a modulating waveform includes one of sinusoidal wave as claimed. However, Prockup does teach this feature in Figures 1, 2 and 3. In Prockup Figure 1, FM modulation circuitry 10 receives an RF carrier signal from RF source 12 as well as a modulating signal from modulation source 14. The modulating waveform from modulating source 14 is shown as a sine wave. (Column 2 lines 63-67) The benefit being that modulation can be accurately generated and measured well below a modulation frequency of 1 Hz. (Column 1 lines 56-59)

18. Therefore, taking the combined teaching and Prockup as a whole, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined teaching to include the modulating waveform of a sine wave as taught by Prockup so that the whole modulation system can be accurately generated and measured well below a modulation frequency of 1Hz.

19. As to claim 5 refer to the combined teaching above. Note also, that Davis discloses an accumulator circuit that includes a digital adder (a 4-bit adder) circuit

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having first and second inputs, a sum output, and a carry output, wherein the digital adder circuit is arranged to receive the modulated waveform signal at the first input, the sum output is coupled to the second input, and wherein the digital adder circuit is configured to provide the carry signal at the carry output. (Davis et al, Column 2 lines 5-18).

20. Claim 6 rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teaching as applied to claim 1 above, and further in view of Watarai US PG Publication 2003/0053577 A1.

21. As to claim 6, refer to the combined teaching above. Note also, that Castiglione teaches the phase detection circuit including a phase detector and a charge pump in Figure 1. Castiglione fails to teach a low-pass filter circuit. However, Watarai does teach this feature. In Watarai the phase control part has functions of phase detect, charge pump and low-pass filter. [paragraph 0028]

22. As to claim 7 refer to the combined teaching above; note that claim 7 is rendered obvious by the combined teaching as taught claim 1 above.

23. Claims 8 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teaching as applied to claim 1 above, and further in view of van Rassel US 4697277.

24. As to claim 8, refer to the combined teaching above. Note too that the combined teaching fails to disclose the modulating waveform signal includes a multiple-bit digital word that varies over time according to the modulating waveform. However, van Rassel does teach this feature. In van Rassel, the first and second waveforms are of the same

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duration and are transmitted in phase with each other; and m and n are positive real numbers, with m greater than one. The second waveform is different from, and preferably negatively correlated with, the first. When the receiver detects a series of first waveforms in the received signal, it locally generates a series of waveforms and correlates the locally-generated signal with the received signal. A change in correlation is detected as the synchronization pulse. (Abstract) At the transmitter, the synchronization pulse whose leading or trailing edge, typically, is used as datum for the various operations is encoded as a series of repeated code patterns (electrical waves) which may be either analog waveforms or digital words. If they are binary digital words, each is preferably the complement of the other. (Column 2 lines 22-39) The advantage being to reliably recover synchronization information from a received signal in the presence of noise. (Column 2 lines 18-21)

25. Therefore, taking the combined teaching and van Rassel as a whole, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined teaching to include the modulating waveform signal that includes a multiple-bit digital word as taught by van Rassel so that the entire system could reliably recover synchronization information from a received signal in the presence of noise.

26. As to claims 9 and 18, refer to the combined teaching above; note that claim 9 is rendered obvious by the combined teaching as taught claim 1 above.

27. Claims 10 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teaching as applied to claim 1 above, and further in view of Bickley US 5152005 A.

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28. As to claim 10, refer to the combined teaching above. The combined teaching fails to disclose that a frequency that is associated with the output clock signal corresponds to a frequency that is associated with the synthesized signal divided by a third number. However, Bickley does teach this feature in Figure 3. According to Bickley, divide-by-N3 circuit 224 has an input 226 connected to the output of VCO 220 for receiving f_3 . The output terminal 228 of divider 224 is connected to another input terminal 230 of phase detector 210. Control terminal of divider 224 is adapted to receive a program 3 for controlling the divisor. (Column 7 lines 54-60) The advantage being to provide simple and inexpensive phase locked loop, frequency synthesizer circuitry for creating a selected one of any of a plurality of chosen discrete frequencies within a predetermined band while enabling the reference frequency to be maintained at relatively high values and still provide a large number of output frequencies. (Column 2 lines 45-51)

29. Therefore, taking the combined teaching and Bickley as a whole, it would have been obvious to one of ordinary skill in the art at time of the invention to modify the combined teaching to include the synthesized signal divided by a third number as taught by Bickley such that a simple and inexpensive phase locked loop and frequency synthesizer circuitry could be provided.

30. Claim 11 rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teaching as applied to claim 1 above, and further in view of US 6580432 B1.

31. As to claim 11 refer to the combined teaching above. Note also that the combined teaching fails to teach the modulating waveform is suitable for spreading a

frequency spectrum that is associated with the synthesized signal relative to a frequency spectrum that is associated with the reference signal according to a downspread modulation. However, Leung does teach this feature. According to Leung, downspread modulation requires a shifting of the carrier frequency down by half of the modulation amount so that the modulate away form is centered on the new carrier. Accordingly, the peak of the modulation is at the original carrier level. One advantage of downspreading is that it can ensure that a system does not exceed the maximum processor's clock speed. (Column 1 lines 50-57)

32. Therefore, taking the combined teaching and Leung as a whole, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined teaching to include the downspread modulation as taught by Leung so that the entire system does not exceed the maximum processor's clock speed.

33. As to claim 12 refer to the combined teaching above; note that claim 12 is rendered obvious by the combined teaching as taught claim 11 above.

34. Regarding claim 13 rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teaching as applied to claim 1 above. Note too that Castiglione teaches a phase detector capable of detecting the phase shift between the first input signal consisting of the divider circuit output signal and a second signal originating form the feedback of the PLL. (Column 3 lines 1-23) Therefore, it would have been obvious to one of ordinary skill in the art that the combined teaching renders the circuit for spread spectrum clock generation of claim 13 obvious.

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35. As to claim 14, refer to the combined teaching above; note that claim 14 is rendered obvious by the combined teaching as taught in claim 13 above.

36. Regarding claim 20 refer to the combined teaching above; note that claim 20 is the corresponding claim to claim 13 and is rendered obvious by the combined teaching as taught claim 13 above.

37.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sonia J. King whose telephone number is 571-270-1307. The examiner can normally be reached on Mon-Fri 7:30am-5pm alt Fri's off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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